BT139X-600E

Triac; sensitive gate

Rev. 4 — 28 October 2011 Product data sheet

1. Product profile

1.1 General description

Passivated, sensitive gate triac in a ‘full pack’ SOT186A (TO-220) plastic package.

1.2 Features and benefits

- High sensitivity in all four quadrants.

1.3 Applications

- General purpose bidirectional switching
- Phase control.

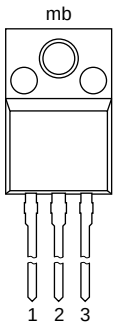
1.4 Quick reference data

- $V_{DRM} \leq 600$ V
- $I_{T(RMS)} \leq 16$ A
- $I_{TSM} \leq 155$ A
- $I_{GT} \leq 10$ mA (T2+ G+; T2+ G–; T2– G–)
- $I_{GT} \leq 25$ mA (T2– G+).

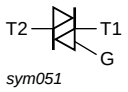
2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	main terminal 1 (T1)		
2	main terminal 2 (T2)		
3	gate (G)		
mb	isolated		



SOT186A (TO-220)



3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BT139X-600E	-	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 'full pack'	SOT186A

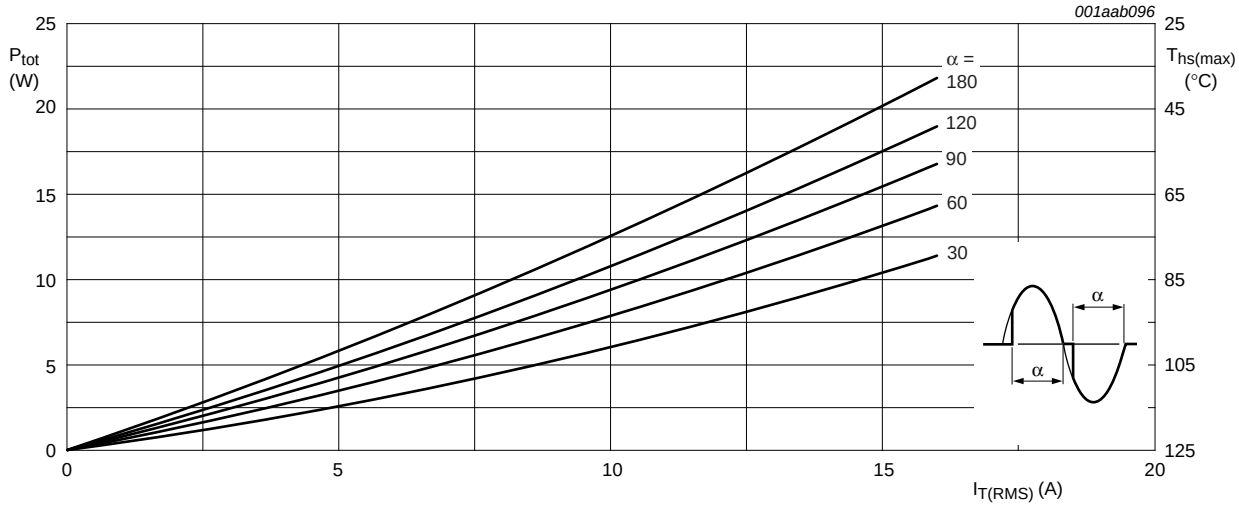
4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

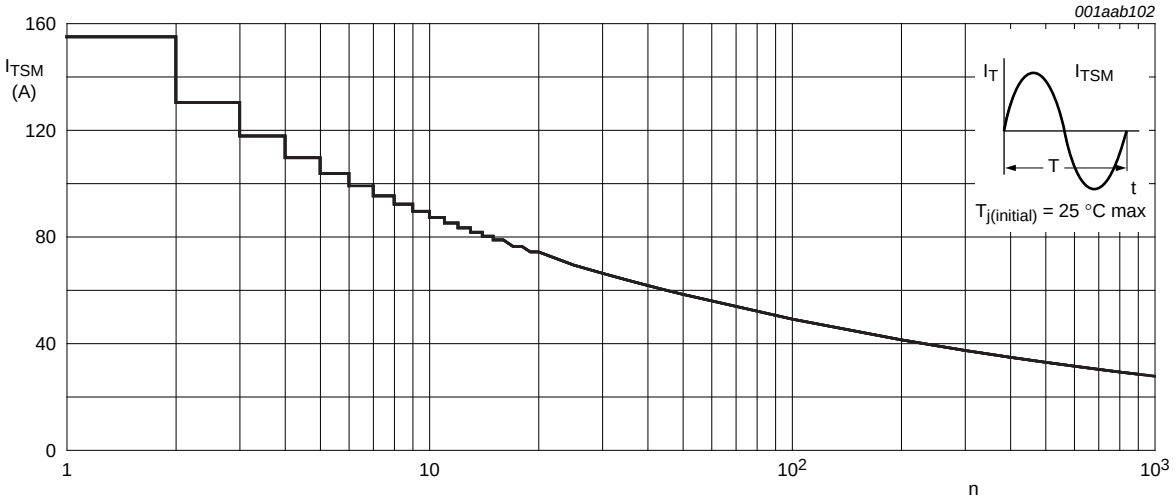
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ °C		-	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge				
		t = 20 ms		-	155	A
		t = 16.7 ms		-	170	A
I^2t	I^2t for fusing	t = 10 ms		-	120	A^2s
dI_T/dt	repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+		-	50	A/µs
		T2+ G–		-	50	A/µs
		T2– G–		-	50	A/µs
		T2– G+		-	10	A/µs
I_{GM}	peak gate current			-	2	A
V_{GM}	peak gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			–40	+150	°C
T_j	junction temperature			-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.



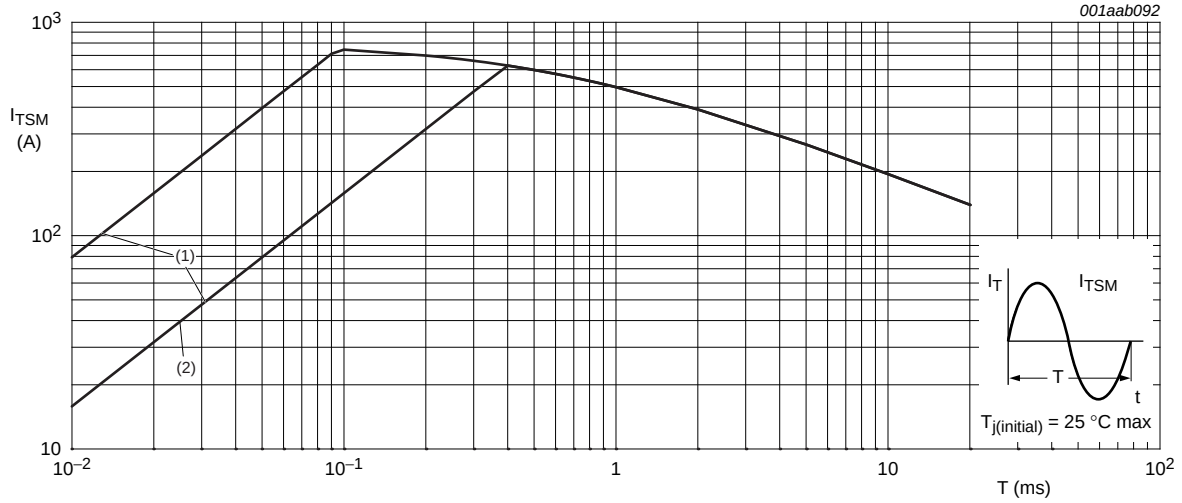
α = conduction angle.

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz.

Fig 2. Non-repetitive peak on-state current as a function of the number (n) of sinusoidal current cycles; maximum values

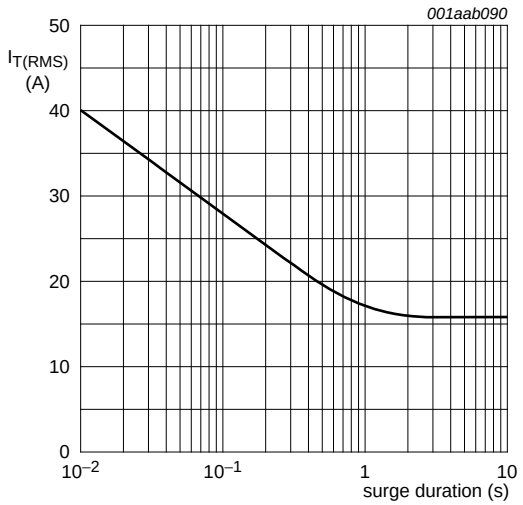


$t_p \leq 20$ ms.

(1) dI_T/dt limit.

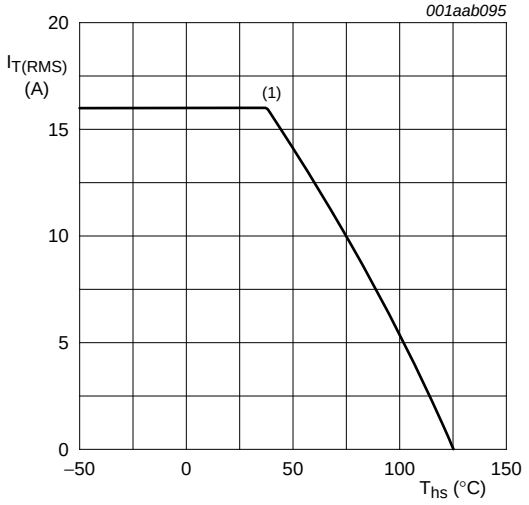
(2) T2– G+ quadrant.

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values



f = 50 Hz; $T_{hs} \leq 38$ °C.

Fig 4. RMS on-state current as a function of surge duration; maximum values



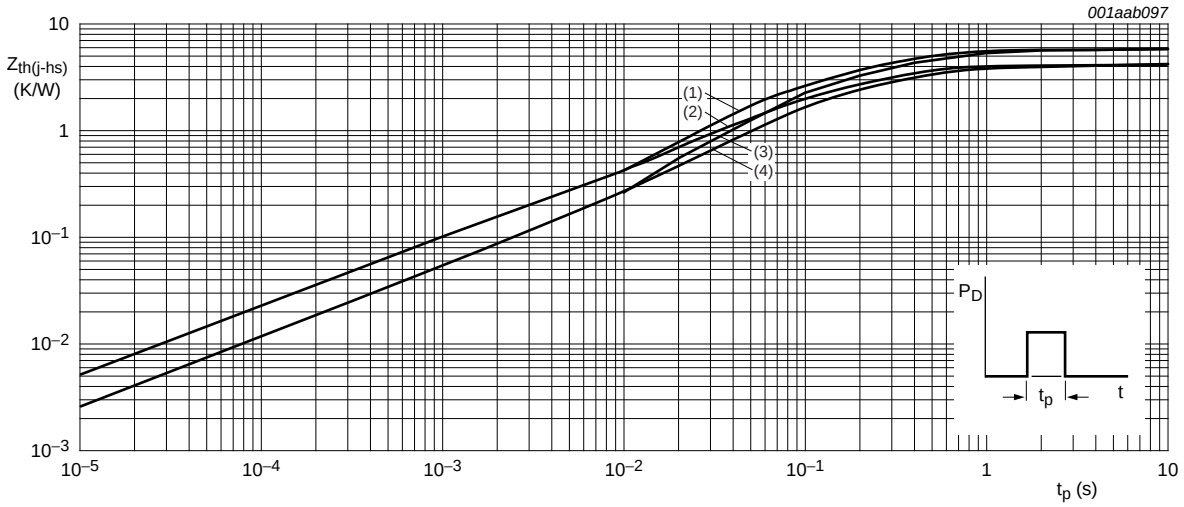
(1) $T_{hs} \leq 38$ °C.

Fig 5. RMS on-state current as a function of mounting base temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-hs)}$	thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	4.0	K/W
		full or half cycle without heatsink compound	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance junction to ambient	in free air	-	55	-	K/W



(1) Unidirectional without heatsink compound.

(2) Unidirectional with heatsink compound.

(3) Bidirectional without heatsink compound.

(4) Bidirectional with heatsink compound.

Fig 6. Transient thermal impedance as a function of pulse width

6. Isolation characteristics

Table 5. Isolation limiting values and characteristics

T_{hs} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{isol}	RMS value isolation voltage from all three terminals to external heatsink	f = 50 to 60 Hz; sinusoidal waveform; R.H. ≤ 65 %; clean and dust free	-	-	2500	V
C_{isol}	capacitance from pin 2 to external heatsink	f = 1 MHz	-	10	-	pF

7. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; Figure 8				
		T2+ G+	-	2.5	10	mA
		T2+ G–	-	4	10	mA
		T2– G–	-	5	10	mA
		T2– G+	-	11	25	mA
I_L	latching current	V_D = 12 V; I_{GT} = 0.1 A; Figure 10				
		T2+ G+	-	3.2	30	mA
		T2+ G–	-	16	40	mA
		T2– G–	-	4	30	mA
		T2– G+	-	5.5	40	mA
I_H	holding current	V_D = 12 V; I_{GT} = 0.1 A; Figure 11	-	4	45	mA
V_T	on-state voltage	I_T = 20 A; Figure 9	-	1.2	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; Figure 7	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-	V
I_D	off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	V_{DM} = 67 % $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

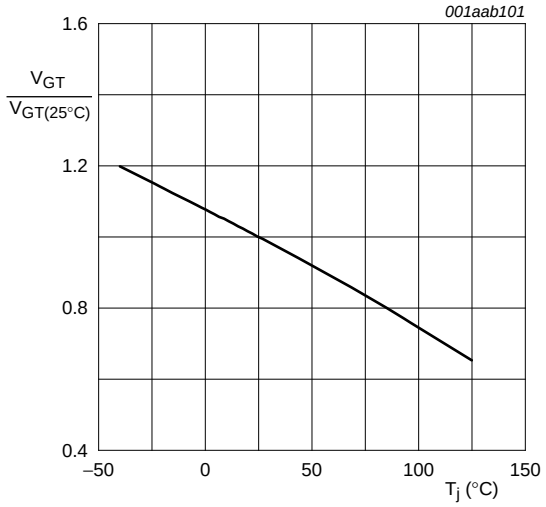
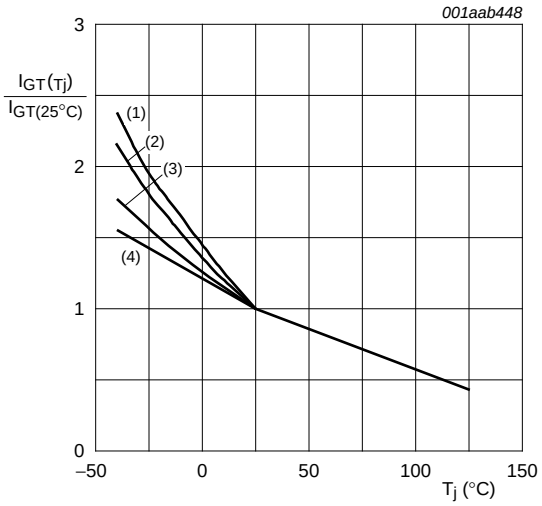


Fig 7. Normalized gate trigger voltage as a function of junction temperature



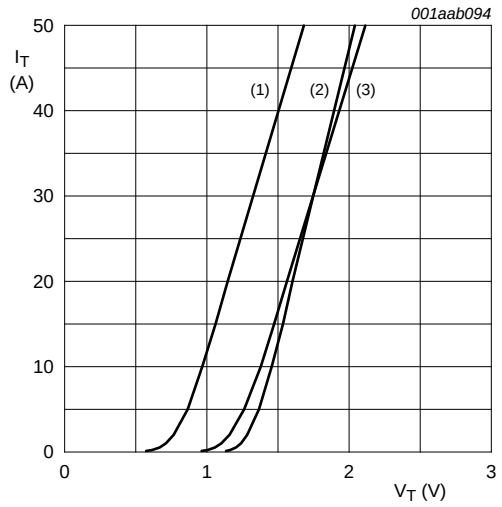
(1) T2– G+.

(2) T2+ G–.

(3) T2– G–.

(4) T2+ G+.

Fig 8. Normalized gate trigger current as a function of junction temperature



V_O = 1.195 V.

R_s = 0.018 Ω.

(1) T_j = 125 °C; typical values.

(2) T_j = 25 °C; maximum values.

(3) T_j = 125 °C; maximum values.

Fig 9. On-state current characteristics

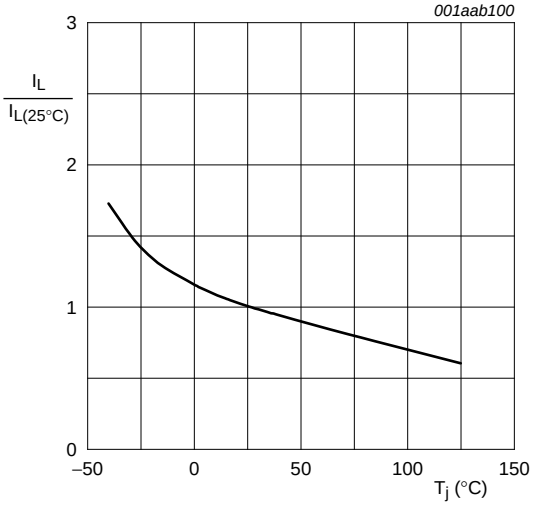


Fig 10. Normalized latching current as a function of junction temperature

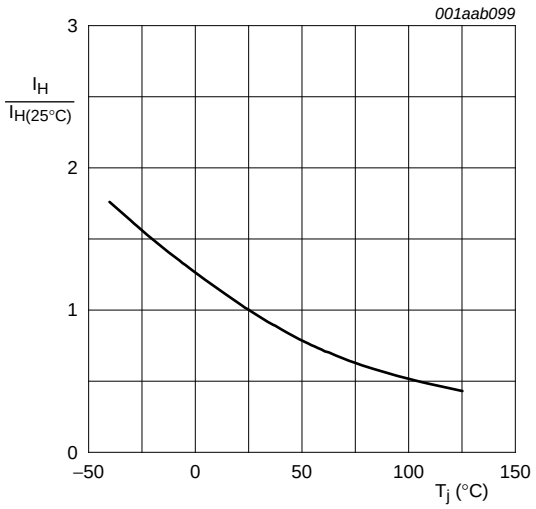


Fig 11. Normalized holding current as a function of junction temperature

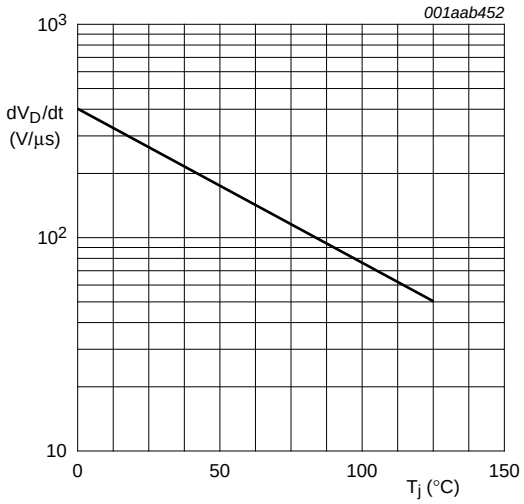


Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

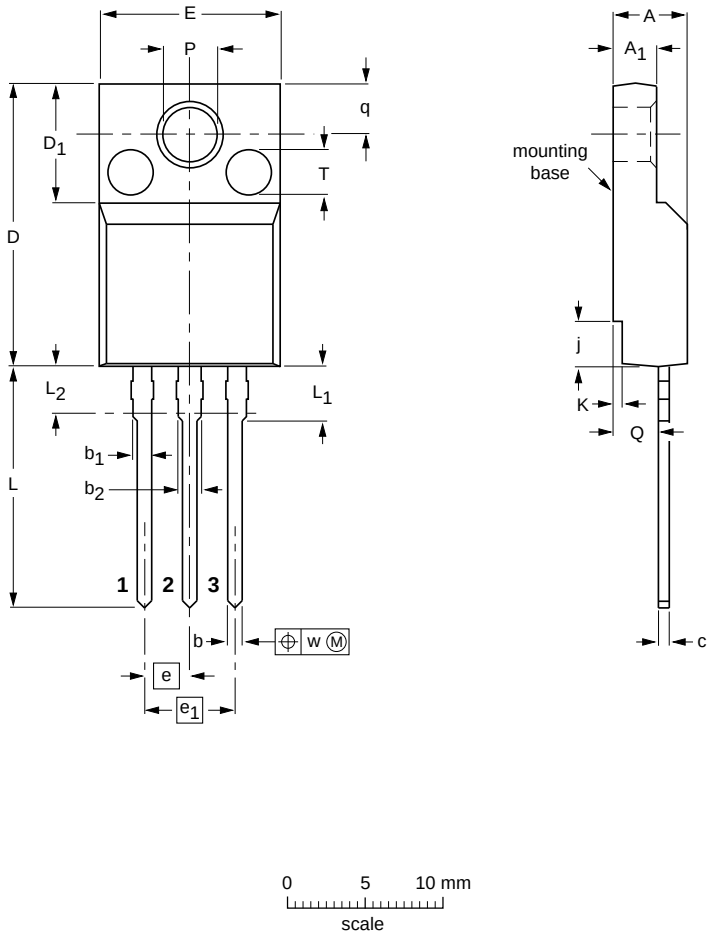
8. Package information

Epoxy meets requirements of UL94 V-0 at $\frac{1}{8}$ inch.

9. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig 13. Package outline; SOT186A (TO-220)

10. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT139X-600E v.4	20111028	Product data sheet		BT139X-600E v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BT139X-600E v.3	20040923	Product data sheet		BT139X-600E v.2
BT139X-600E v.2	20011001	Product specification		BT139X_SERIES_E v.1
BT139X_SERIES_E v.1	19970901	Product specification		-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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